CLAIMS

1. A method of forming an active device, the method comprising:

performing a first patterning operation on a first plurality of layers, the first patterning operation defining a first feature of the active device; and

performing a second patterning operation on at least one patterned layer of the first plurality of layers, the second patterning operation defining a second feature of the active device, wherein the first and second patterning operations are performed substantially back-to-back.

2. The method of Claim 1, wherein the first patterning operation includes:

etching the first plurality of layers into a first plurality of strips oriented in a first direction.

3. The method of Claim 2, wherein the second patterning operation includes:

etching at least one strip of the first plurality of strips in a second direction, the second direction being different than the first direction, to create a pillar.

4. The method of Claim 3, wherein at least one strip of the first plurality of strips comprises a first terminal of the active device.

5. The method of Claim 4, wherein the pillar comprises another portion of the active device.

6. The method of Claim 4, further including:

depositing a first dielectric after both first and second patterning operations; and

planarizing the first dielectric to expose a surface of the active device.

7. The method of Claim 6, further including performing a cleaning step after planarizing.

8. The method of Claim 6, further including:

depositing a second plurality of layers on the surface of the active device and the first dielectric; and

etching the second plurality of layers into a second plurality of strips oriented in the second direction.

9. The method of Claim 8, wherein said second plurality of strips is not self-aligned to the pillar.

10. The method of Claim 8, wherein at least one strip of the second plurality of strips comprises a second terminal of the active device.

11. The method of Claim 1, wherein the first plurality of layers includes an antifuse layer fully etched through by the first patterning operation, but not fully etched through by the second patterning operation.

12. The method of Claim 1, wherein the first plurality of layers includes an antifuse layer fully etched through by both the first and second patterning operations.

13. A method of forming diodes in an array, the method comprising:

performing a first patterning operation on a first plurality of layers, the first plurality of layers including at least one of a P-type layer and an N-type layer, the first patterning operation forming a first plurality of strips; and

performing a second patterning operation on at least one layer of the first plurality of strips, wherein the first and second patterning operations are performed substantially back-to-back.

14. The method of Claim 13, wherein the first plurality of strips are oriented in a first direction.

15. The method of Claim 14, wherein during the second patterning operation at least one of the first plurality of strips is etched in a second direction, the second direction being different than the first direction.

16. The method of Claim 15, wherein the first plurality of strips include first terminals of the diodes.

17. The method of Claim 15, wherein unetched strips of the first plurality of strips comprise a portion of the diodes and etched strips of the first plurality of strips comprise another portion of the diodes.

18. The method of Claim 16, further including:

depositing a first dielectric after first and second patterning operations; and

planarizing the first dielectric to expose a surface of the diodes.

19. The method of Claim 18, further including performing a cleaning step following planarization.

20. The method of Claim 18, further including:

depositing a second plurality of layers on the surface of the diodes and the first dielectric; and

etching the second plurality of layers into a second plurality of strips oriented in the second direction.

21. The method of Claim 20, wherein the second plurality of strips include second terminals of the diodes.

22. The method of Claim 14, wherein the first plurality of layers includes an antifuse layer fully etched through by the first patterning operation, but not fully etched through by the second patterning operation.

23. The method of Claim 14, wherein the first plurality of layers includes an antifuse layer fully etched through by the first and second patterning operations.

24. The method of Claim 21, wherein the array is a three-dimensional array and a portion of the second plurality of strips is etched in the first direction to form another plane of diodes.

25. An incipient diode structure including vertically formed diodes, the structure comprising:

a first set of strips including a first terminal and a first portion of a first diode;

a first pillar including a second portion of the first diode;

a second set of strips including a common terminal shared by the first diode and a second diode;

a second pillar including a first portion of the second diode; and

a third set of strips including a second portion of the second diode and another terminal of the second diode, wherein each of the pillars is substantially free of stringers.

26. The incipient diode structure of Claim 25, wherein the first set of strips includes:

a first heavily doped silicon strip of a first type;

a first conductive strip formed on the first heavily doped silicon strip;

a second heavily doped silicon strip of the first type formed on the first conductive strip; and

an antifuse strip formed on the second heavily doped silicon strip.

27. The incipient diode structure of Claim 26, wherein the first pillar includes:

a first silicon pillar structure of a first type formed on the antifuse strip.

28. The incipient diode structure of Claim 27, wherein the second set of strips includes:

a third heavily doped silicon strip of the second type formed on the first silicon pillar structure; and

a second conductive strip formed on the third heavily doped silicon strip.

29. The incipient diode structure of Claim 28, wherein the second pillar includes:

a first heavily doped silicon pillar structure of the second type formed on the second conductive strip;

a second silicon pillar structure of the second type formed on the first heavily doped silicon pillar structure;

a third heavily doped silicon pillar structure of the first type formed on the second silicon pillar structure; and

an antifuse pillar structure formed on the third silicon pillar structure.

30. The incipient diode structure of Claim 29, wherein the third set of strips includes:

a fourth heavily doped silicon strip of the first type formed on the antifuse pillar structure; and

a third conductive strip formed on the fourth heavily doped silicon strip.

31. The incipient diode structure of Claim 30, wherein the first, second, and third conductive strips include a refractory metal.

32. The incipient diode structure of Claim 31, wherein the antifuse strip includes deposited silicon dioxide.

33. The incipient diode structure of Claim 32, wherein the antifuse pillar structure is grown with rapid thermal oxidation (RTO).

34. A method of forming a pillar from a plurality of layers formed on a wafer, the method comprising:

performing substantially back-to-back patterning steps,

wherein a first patterning step etches a plurality of layers in a first direction, thereby forming patterned structures,

wherein a second patterning step etches the patterned structure in a second direction, and

wherein the first direction is different from the second direction.

35. A method of forming an active device, the method comprising:

performing a first patterning operation on a first plurality of layers, the first patterning operation defining a first terminal of the active device;

performing a second patterning operation on at least one patterned layer of the first plurality of layers, the second patterning operation defining a first feature of the active device, wherein the first and second patterning operations are performed substantially back-to-back; and

performing a third patterning operation on a second plurality of layers, wherein the third patterning operation defines a second feature and a second terminal of the active device.

36. The method of Claim 35, wherein the first patterning operation includes:

etching the first plurality of layers into a first plurality of strips oriented in a first direction.

37. The method of Claim 36, wherein the second patterning operation includes:

etching at least one of the first plurality of strips in a second direction, the second direction being different than the first direction, to define the first feature.

38. The method of Claim 37, further including:

depositing a first dielectric after both first and second patterning operations; and

planarizing the first dielectric to expose a surface of the active device.

39. The method of Claim 38, wherein performing the third patterning operation is preceded by steps including:

depositing a second plurality of layers on the surface of the active device and the first dielectric; and

etching the second plurality of layers into a second plurality of strips oriented in the second direction.

40. The method of Claim 39, wherein at least one strip of the second plurality of strips comprises the second feature, and wherein at least one other strip of second plurality of strips comprises the second terminal of the active device.

41. The method of Claim 38, further including growing antifuse material on the exposed surface of the active device.

42. A method of forming diodes in an array, the method comprising:

performing a first patterning operation on a first plurality of layers, the first plurality of layers including a first silicon-type layer, the first patterning operation forming a first plurality of strips; and

performing a second patterning operation on at least one layer of the first plurality of strips, the second patterning operation defining one feature of a plurality of diodes from the first silicon-type layer, wherein the first and second patterning operations are performed substantially back-to-back.

43. The method of Claim 42, wherein the first plurality of strips are oriented in a first direction.

44. The method of Claim 43, wherein during the second patterning operation at least one of the first plurality of strips is etched in a second direction, the second direction being different from the first direction.

45. The method of Claim 42, wherein the first plurality of strips include first terminals of the diodes.

46. The method of Claim 45, further including:

depositing a first dielectric after first and second patterning operations; and

planarizing the first dielectric to expose a surface of the diodes.

47. The method of Claim 46, further including performing an HF dip following planarizing.

48. The method of Claim 46, further including:

depositing a second plurality of layers on the surface of the diodes and the first dielectric; and

etching the second plurality of layers into a second plurality of strips oriented in the second direction.

49. The method of Claim 48, wherein the second plurality of strips include second features and second terminals of the diodes.

50. The method of Claim 46, further including growing antifuse material on the exposed surfaces of the diodes.

51. The method of Claim 48, wherein the array is a three-dimensional array and a portion of the second plurality of strips are etched in the first direction to form features of another plane of diodes.

52. A method of isolating pillars on an integrated circuit, the method including:

performing a first anisotropic etch on a first plurality of layers, thereby forming patterned structures; and

performing a second anisotropic etch on the patterned structures, thereby forming the functional pillars, wherein the first and second anisotropic etches are performed substantially back-to-back.

53. The method of Claim 52, wherein the first plurality of layers includes at least one silicon-type layer.

54. The method of Claim 52, wherein the first plurality of layers includes at least one refractory metal layer.

55. The method of Claim 52, wherein the first plurality of layers includes an antifuse layer.

56. A method of forming diodes in an array, the method comprising:

performing a first patterning operation on a first plurality of layers, the first plurality of layers including an N layer and two P+ layers sandwiching an antifuse layer, the first patterning operation forming a first plurality of strips; and

performing a second patterning operation on at least the N layer of the first plurality of strips, wherein the first and second patterning operations are performed substantially back-to-back.

57. The method of Claim 56, wherein the first plurality of strips are oriented in a first direction.

58. The method of Claim 57, wherein during the second patterning operation at least the N layer is etched in a second direction, thereby forming a pillar, wherein the second direction is different than the first direction.

59. The method of Claim 58, wherein the first plurality of strips include first terminals of the diodes.

60. The method of Claim 59, wherein unetched strips of the first plurality of strips comprise first terminals of the diodes and etched strips of the first plurality of strips comprise at least a portion of the diodes.

61. The method of Claim 60, further including:

depositing a first dielectric after first and second patterning operations; and

planarizing the first dielectric to expose a surface of the diodes.

62. The method of Claim 61, further including performing a cleaning step following planarization.

63. The method of Claim 61, further including:

depositing a second plurality of layers on the surface of the diodes and the first dielectric; and

etching the second plurality of layers into a second plurality of strips oriented in the second direction.

64. The method of Claim 63, wherein the second plurality of strips include second terminals of the diodes.

65. The method of Claim 56, wherein the first plurality of layers includes the antifuse layer fully etched through by the first patterning operation, but not fully etched through by the second patterning operation.

66. The method of Claim 56, wherein the first plurality of layers includes the antifuse layer fully etched through by the first and second patterning operations.

67. The method of Claim 64, wherein the array is a three-dimensional array and a portion of the second plurality of strips are etched in the first direction to form another plane of diodes.

68. A monolithic 3-dimensional memory array comprising:

a first set of strips including a first terminal;

a second set of strips including a second terminal;

a third set of strips including a third terminal;

a first pillar having at least one side wall with a slightly positive slope, said pillar disposed between and connecting said

first and second sets of strips, and including a first P doped silicon region, a first N doped silicon region and a first insulating region;

a second pillar having at least one side wall with a slightly positive slope, said pillar disposed between and connecting said second and third sets of strips, and including a second P doped silicon region, a second N doped silicon region and a second insulating region;

wherein each of the pillars is substantially free of stringers.

69. The memory of Claim 68, wherein each of said first and second insulating regions is disposed between the respective P and N doped silicon regions.

70. The memory of Claim 68, wherein the respective P and N doped silicon regions abut one another.